CLAIMS

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1. A resource access control mechanism for a computer system including at least one central processing unit, the resource access control mechanism comprising an address translation mechanism operable to map a received address to a resource and a trap handler for handling a trap in the event of a faulty resource access being detected, the trap handler being operable to instigate a diversion for subsequent access attempts to the resource and the address translation mechanism being responsive to instigation of a diversion by the trap handler to effect the diversion for subsequent attempts to access the resource.

2. The resource access control mechanism of claim 1, wherein the trap handler is further operable to process an exception.

3. The resource access control mechanism of claim 1 or claim 2, wherein the address translation mechanism includes a translation look-aside buffer.

4. The resource access control mechanism of any preceding claim, wherein the address translation mechanism forms part of a memory management unit.

5. The resource access control mechanism of any preceding claim, wherein the trap handler is operable to identify an alternative resource address to the address translation mechanism for replacing a resource address held in an address translation entry for the resource.

6. The resource access control mechanism of any of claims 1 to 4, wherein the trap handler is operable to instigate the diversion by signaling the address translation mechanism.

7. The resource access control mechanism of claim 6, wherein the address translation mechanism is responsive to instigation of a diversion by the trap handler to replace a resource address held in an address translation entry for the resource with an alternative resource address.

8. The resource access control mechanism of claim 6, wherein the address translation mechanism is responsive to instigation of a diversion by the trap handler to set a divert flag in a translation entry of the address translation and is further operable to respond to a received address relating to an address translation entry having a divert flag set to use an alternative address to that held in the address translation entry.

9. The resource access control mechanism of claim 6, wherein the address translation mechanism is responsive to instigation of a diversion by the trap handler to set a divert flag in a translation entry of the address translation and is further operable to respond to a received address relating to an address translation entry having a divert flag set to modify an address held in the address translation entry.

10. The resource access control mechanism of any preceding claim, wherein the resource is at least one memory location.

11. The resource access control mechanism of any of claims 1 to 9, wherein the resource is a peripheral device.

12. The resource access control mechanism of any of claims 1 to 9, wherein the resource is a subsystem.

13. The resource access control mechanism of any preceding claim, wherein the alternative resource is a faked response generator.

14. The resource access control mechanism of any of claims 1 to 12, wherein the alternative resource is a predefined memory portion.

15. A computer system comprising at least one processor that includes at least one central processing unit, memory, at least one peripheral device and the resource access control mechanism of any preceding claim.

16. The computer system of claim 15, operable to identify an initial faulty access to a resource.

17. A method of managing processor access to resources in a computer system, the method comprising:
handling a trap in the event of an initial faulty access attempt to a resource being detected;
defining a diversion for subsequent access attempts to the same resource;
diverting a subsequent attempt to access the resource.

18. The method of claim 17, further comprising processing an exception.

19. The method of claim 17 or claim 18, wherein the defining of a diversion includes replacing a resource address held in an address translation entry for the resource with an alternative resource address.

20. The method of claim 17 or claim 18, wherein the defining of a diversion includes setting a divert flag in an address translation entry for the resource and the diverting of a subsequent attempt to access the resource includes using

an different address to that held in the address translation entry when the divert flag is set.

21. The method of claim 17 or claim 18, wherein the defining of a diversion includes setting a divert flag in an address translation entry for the resource and the diverting of a subsequent attempt to access the resource includes modifying an address held in the address translation entry.

22. The method of any of claims 17 to 21, wherein the diversion is to a predefined memory portion.

23. The method of any of claims 17 to 21, wherein the diversion results in the generation of a faked response to the resource access.

24. The method of any of claims 17 to 23, wherein the resource is at least one memory location.

25. The method of any of claims 17 to 23, wherein the resource is a peripheral device.

26. The method of any of claims 17 to 23, wherein the resource is a subsystem.

27. A computer program forming a trap handler for a computer system according to claim 15, the computer program comprising computer code operable:
to respond to a faulty resource access by processing an exception; and
to instigate a diversion in an address translation mechanism for subsequent access attempts to the resource.

28. A computer program product comprising the computer program of claim 23, wherein said program code is carried by a carrier medium.